**BSc Project Title:**
"RISC-V synthesis and programming"

**Abstract:**
The project will explore and evaluate the possibilities offered by the RISC-V ecosystem [1]. This type of architecture will be synthesized on hardware (FPGA) and one or several software programs will be developed for it and tested on the FPGA.

**Possible tasks (depending on the skills and ambition of the student):**

- Survey of existing RISC-V cores;
- Selection of a RISC-V core and synthesis thereof on FPGA;
- Selection or design of one or several software programs (e.g. common benchmarks or own idea);
- Software implementation of the above.

**Prerequisites:**
Knowledge of embedded systems including microprocessor (soft) cores and FPGAs, programing skills (e.g. C/C++)

**References:**
[1] RISC-V webpage. [Online] https://riscv.org/. Visited on 05-Sept. 2021

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